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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/034,236	12/28/2001	Philip J. Ireland	11675.99.2	9992
24247	7590	02/14/2006	EXAMINER	
TRASK BRITT P.O. BOX 2550 SALT LAKE CITY, UT 84110			TSAI, H JEY	
			ART UNIT	PAPER NUMBER
			2812	

DATE MAILED: 02/14/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claim 43 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Gardner et al., 5,973,910, cited by applicants.

Gardner method of fabricating an integrated circuit that includes a semiconductor substrate 100 having an active region 100 therein, a capacitor storage node 102 upon the active region 100, a capacitor dielectric layer 103 upon the capacitor storage node 102, a cell plate conductor layer 104 upon the capacitor dielectric layer 103, a cell plate insulator layer 105 upon the cell plate conductor layer 104, the method comprising:

forming a contact hole extending through the cell plate insulator layer 105, the cell plate conductor layer 104, the capacitor dielectric layer 103, and the capacitor storage node 102 to terminate at the

active region, 100, fig. 1A-1B and col. 3, line 33 to col. 4, line 67,

forming a sleeve insulator layer 107 within the contact hole, the

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sleeve insulator layer extending from a terminus at an interface between the cell plate insulator layer 105 and an opposite terminus that is below the capacitor dielectric layer 103 and above the semiconductor substrate1, fig. 1E,

forming an electrically conductive plug extending through the sleeve insulator layer to make contact with the active region and the capacitor storage node, the electrically conductive plug being electrically insulated from the cell plate conductor layer by the sleeve insulator layer.

Allowable Subject Matter

Claims 1-42 are allowable over the prior art of record for the reason of forming an opening terminating at a bottom surface within the lower bulk insulator layer and the thickness of the upper bulk insulator layer is greater than the thickness of the cell plate insulator layer.

Conclusions

Applicant's arguments filed Dec. 1, 2005 have been fully considered but they are not persuasive. Because there is not seen that the word "above" precludes the sleeve insulator from contacting the semiconductor substrate.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

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A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry of a general nature or clerical matters or relating to the status of this application or proceeding should be directed to the customer service whose telephone number is (703) 308-4357.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to H. Jey Tsai whose telephone number is (571) 272-1684. The examiner can normally be reached on from 7:00 Am to 4:00 Pm., Monday thru Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael S. Lebentritt can be reached on (571) 272-1873.

The fax phone number for this Group is (703) 872-9306.

hjt

2/2/2006



H. Jey Tsai

Primary Examiner
Patent Examining Group 2800